InGaAs Inversion Layer Mobility and Interface Trap Density from Gated Hall Measurements

T. Chidambaram, D. Veksler, S. Madisetti, M. Yakimov, V. Tokranov, and S. Oktyabrsky

Abstract— **In this work, we use gated Hall method for direct measurement of free carrier density and electron mobility in inversion InGaAs MOSFET channels. At room temperature, the highest Hall mobility of 1800 cm^2/Vs is observed at electron density in the channel ≈1x10^{12} cm^{-2}. A comparison with mobility values estimated from transistor characteristics reveals a significant underestimation of mobility which arises from overestimation of channel density obtained from C-V measurements. Temperature dependence of the electron mobility provides the evidence that remote Coulomb scattering dominates at electron density < 3x10^{11} cm^{-2}. Contrary to the capacitance-based methods commonly used for extraction of interface trap density, gated Hall method can separate the contributions of fast-trapped charges and free carriers in the channel to the total charge of a MOS capacitor. This allows for reliable estimation of trap density at the III-V/high-k interface including border traps. The results illustrate that even high-quality interfaces providing high-mobility transport suffer from fast border traps above the conduction band. In contrast with Si where the effect of border traps is negligible, in low density-of-state InGaAs channel material as much as half of the channel electrons can be trapped and excluded from transport, increasing switching energy and dissipated power.**

***Index Terms*—III-V MOSFETs, interface states, mobility, carrier density, scattering mechanism**

I. INTRODUCTION

GROUP III-V semiconductors are potential candidates for replacement of Si channel for complimentary metal-oxide-semiconductor (CMOS) logic applications because of. their high carrier mobility. However, reduction of electron trap density at high-k oxide/III-V interface is still the major challenge for III-V device technology in sub 10nm nodes [1,2]. Conventional characterization methods primarily based on admittance measurements are unable to unambiguously determine interface trap density (D_{it}) [3-8]; in particular, they cannot distinguish between free carriers and trapped carriers with fast response. In addition, III-V materials have low density of conduction band states and relatively high density of border traps [9,10] that can have very fast (up to GHz) response [11] contributing to C-V measurements even under strong inversion conditions in contrast with Si MOS structures. Conventional methods employing a combination of C-V and I-V characteristics to estimate the effective mobility in the channel [5,6,12-15] result in over-estimation of channel charge thereby leading to under-estimation of carrier mobility. In this work, we use a gated Hall method to find the mobility and D_{it} in an $In_{0.53}Ga_{0.47}As$ inversion channel. Gated Hall method [12, 16-19] extracts D_{it} without assumption of the trapping rates and the mobility is obtained from the Hall/conductivity measurements. Previously, we used gated Hall method to extract D_{it} and mobility in buried InGaAs channels [17-19].

II. INGAAS GATED HALL STRUCTURE

An inversion MOS gated Hall structures with 200 nm thick p-$In_{0.53}Ga_{0.47}As$ (Carbon doped, 1x10^{17} cm^{-3}) layer and 50 nm n^+-$In_{0.66}Ga_{0.34}As$/InAs, (Si doped, 5x10^{19} cm^{-3}) contact layer were grown by molecular beam epitaxy on semi-insulating (SI) InP substrate (Fig. 1a). Fabrication of the gated Hall devices included four lithographic steps. Firstly, devices are isolated by dry etching (methane-hydrogen plasma) down to about 100 nm below the channel. In the next step, the contact layer is etched using methane-hydrogen plasma, and the channel surface is cleaned by in a 2:1 HCl:H_2O solution. Before depositing Al_2O_3, the p-InGaAs surface is passivated by a quick (1 s to 2 s) dip in a concentrated HCl. A 10 nm thick Al_2O_3 layer is grown using atomic layer deposition (ALD) in 90 cycles at 350˚C with trimethylaluminium and water as precursors, followed by TiW gate metal sputtering. Finally Pd/Ge Ohmic contacts are e-beam evaporated onto a n+InGaAs surface cleaned with 1:1 HCl:H_2O, lifted off and annealed in forming gas at 350 ˚C for 10 min. Gated Hall structures were fabricated in Van der Paw (VdP) geometry (Fig. 1a) and in a double Hall-cross bar configuration. In the VdP structures, the potential drop along the length of the channel is much less than in double Hall cross geometry. Thus the VdP geometry allows for more accurate measurement of the carrier density and sheet resistivity in the sub-threshold region. Along with the Hall structures, regular MOSFETs with 7 μm gate lengths were fabricated on the same wafer. The structures were packaged, wire-bonded, and placed in the cryostat for low temperature measurements. Hall and resistivity data were obtained in the temperatures range of 77 K to 300 K in a magnetic field up to 1 T.

III. RESULTS AND DISCUSSION

Free carrier density and sheet resistivity in the channel as a function of gate bias are plotted in Fig. 1(b,c). The dependence of Hall mobility on sheet electron density extracted from the presented data is shown in Fig. 2. Peak values of 1800 cm^2/Vs and 3700 cm^2/Vs are observed at $n_s \approx 1x10^{12}$ cm^{-2} at 300 K and 77 K, respectively. These values are relatively high for the inversion InGaAs layer indicating overall high interface

Manuscript received XXXXX. This work was supported by CNSE-SEMATECH.

T. Chidambaram, S. Madisetti, M. Yakimov, V. Tokranov, and S. Oktyabrsky are with the SUNY Polytechnic Institute, Albany, NY 12203, USA (email: soktyabrsky@sunypoly.edu)
D. Veksler is with NIST, Gaithersburg, MD 20899.

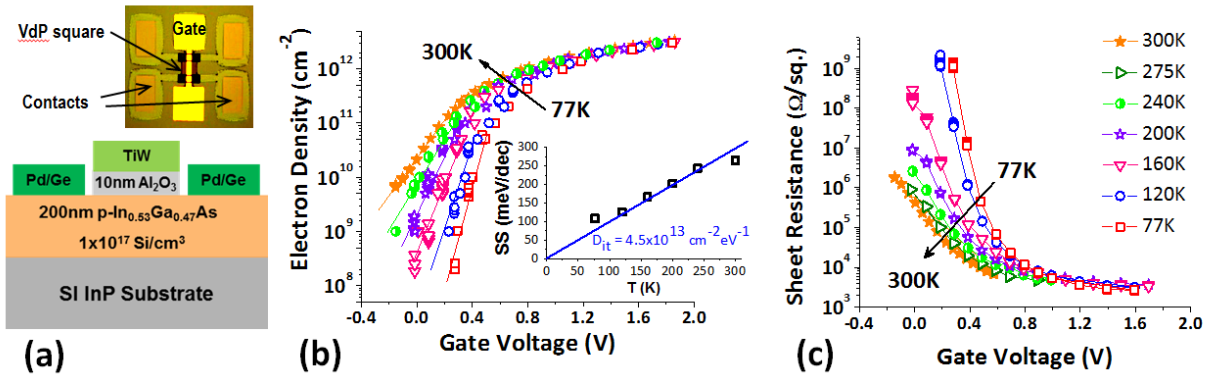

Fig. 1. (a) Cross-section of a gated Hall structure with 200 nm p-$In_{0.53}Ga_{0.47}As$ channel and top view of a trench-isolated 40 x 40 μm^2 Van der Paw device. (b) Electron density, and (c) Sheet resistance as a function of gate bias for the temperature range 77-300 K obtained using Hall measurements. The inset shows the evolution of subthreshold swing (SS) with temperature. The interface traps densities corresponding to the solid line is 4.5x10^{13} cm^{-2}eV^{-1}; qD_{it}=(SS/[ln(10) kT/q] -1)C_{ox} , with C_{ox}=0.8 μF/cm^2.

quality, and match well to the Hall mobilities obtained in gateless InGaAs surface channels [17,20]. It is therefore instructive to analyze D_{it} at this interface. At concentration, n_s > 3x10^{11} cm^{-2}, the electron mobility increases with temperature reduction. This behavior implies metal-oxide interface roughness scattering as the major mobility-limiting mechanism [14,17]. It should be noted that Hall mobility is typically less than drift mobility; the ratio is given by Hall factor. For roughness scattering, the Hall factor is about 1.2 to 1.3 at room temperature [21], and the peak channel effective mobility in this structure is about 1400 cm^2/Vs at 300 K.

At low electron densities, the mobility decreases significantly due to reduction of screening of scattering potential and is strongly affected by remote Coulomb scattering (RCS). At densities < 2x10^{11} cm^{-2}, the dependence of mobility vs. temperature is reversed (Fig. 2), and becomes dominated by RCS [15,19]. This behavior is similar to that observed in the depletion mode $In_{0.53}Ga_{0.47}As$ QW channels [22].

The effective mobility extracted from transistor characteristics employing traditional integration of C-V curves (Fig. 2) is significantly less than measured Hall mobility. This discrepancy results from overestimation of carrier density, caused by charges captured by both interface and border traps. Fig. 3 illustrates the over-estimated inversion channel electron density obtained from transistor split C-V characteristics with that from Hall measurements and projected ideal MOS density from a Schrödinger-Poisson (S-P) simulation. It is important to note that extraction of the channel density by subtracting the interface trap charge (from D_{it} analysis) from the total charge (obtained from C-V integration) [5, 6, 14, 22] recovers the mobile charge only partially. Fast interface and border traps cannot be separated from the mobile charge by this method, while Hall data directly provides free electron concentration ("Hall" curve in the Fig. 3). Differentiation of the carrier density with respect to the gate voltage gives the capacitance of the free electrons in the channel (Fig. 4). The difference of C_{ch} from the measured split C-V characteristics (Fig. 4) is due to the interface charge and can be also used to find the trap density.

D_{it} is extracted from Hall data using two approaches (Fig. 5). The first method compares carrier densities (Fig. 3) obtained from the gated Hall measurements and S-P simulation as originally proposed by Fang and Fowler [12] (SP/Hall in Fig. 5):

$$q_0 D_{it} = C_{ox}\left(\Delta V_{G,\exp} - \Delta V_{G,sim}\right)/\Delta\varphi_s , \qquad (1)$$

where q_o is electron charge, $\Delta\varphi_s$ is the change of the surface potential corresponding to the change of experimental, $\Delta V_{G,exp}$, and ideal, $\Delta V_{G,sim}$, gate voltages at the same channel carrier densities.

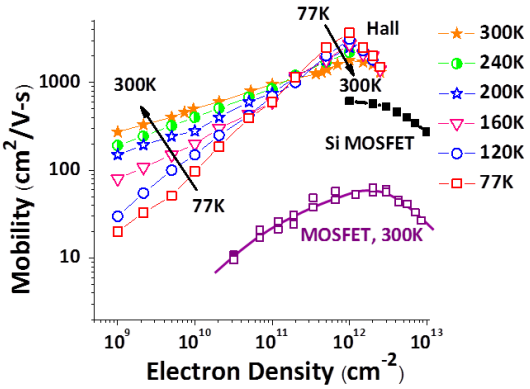

Fig. 2. Comparison of Hall mobility in InGaAs channel at 77 K to 300 K and from split C-V method and InGaAs MOSFET characteristics at 300 K. Universal Si mobility as a function of electron density is shown for reference.

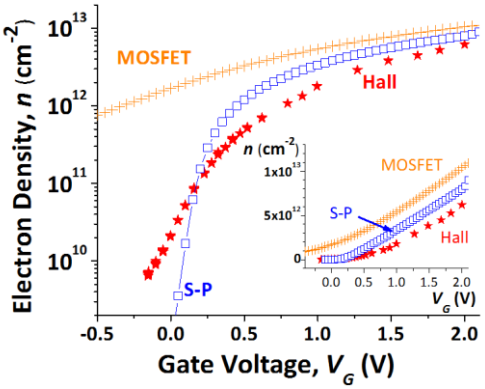

Fig. 3. Comparison of electron density obtained from integration of split C-V characteristics of a MOSFET shown in Fig. 5, Hall measurements and S-P simulation as a function of gate voltage. Inset: linear plot showing ≈2x difference in Hall and C-V densities.

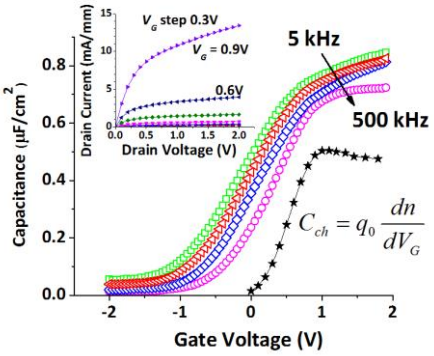

Fig. 4. Experimental capacitance-voltage characteristics measured at different frequencies and channel capacitance C_{ch} obtained from room temperature Hall measurements. Inset: Output characteristics of a MOSFET with gate length 7 μm.

The second method [18,19] utilizes comparison of the channel capacitance, C_{ch}, with the measured MOS capacitance, $C_{exp}(f)$ (Fig. 5) (CV/Hall method):

$$q_0 D_{it}(\varphi_s, f) = \left[C_{\exp}(V_G, f) - C_{ch}(V_G) \right] \Big/ \frac{d\varphi_s}{dV_G}, \qquad (2)$$

with $$\frac{d\varphi_s}{dV_G} = \left(\frac{d\varphi_s}{dV_G} \right)_{SP} \frac{(dn/dV_G)_{Hall}}{(dn/dV_G)_{SP}}$$

calculated from the S-P simulation and Hall electron density vs. gate voltage curve, $n(V_G)$. The extracted density of interfacial traps (D_{it}) also include densities of bulk oxide and border traps, projected to the interface. At a specific C-V measurement frequency, f, the extracted D_{it}, will contain all the traps responding faster than f. The slower traps (for example, those located too deep in the dielectric), which do not respond in C-V measurements, would not be taken into account. Accordingly, the extracted D_{it} distributions exhibit higher values when a lower frequency C-V curve is used (Fig. 5).

Al_2O_3/InGaAs interface has significantly less D_{it} as compared to HfO_2/InGaAs interface [16, 18, 20]. However, D_{it} inside the conduction band (CB), associated with the border traps, is still high. Some of these border traps are likely located within only Angstroms from the oxide/semiconductor interface and have very fast response rates [11] making them indistinguishable from free channel electrons at typical C-V measurement frequencies. Due to the low conduction band density of states, these traps in our high-mobility sample capture almost half of the carriers as evidenced from the Fig. 3. These traps can strongly increase parasitic power dissipation in InGaAs MOSFETs.

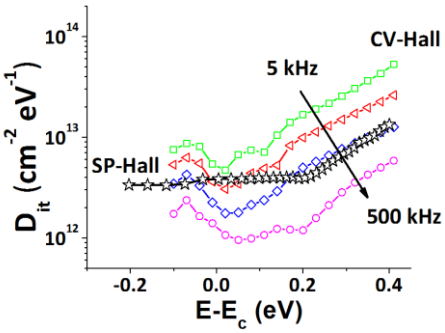

Fig. 5. Interface trap density D_{it} as a function of surface potential extracted from gated Hall measurements using two approaches as described in the text: SP-Hall (stars) and CV-Hall (symbols match C-V curves at different frequencies in Fig. 4).

IV. Conclusions

Gated Hall method allows for reliable extraction of electron density in the inversion InGaAs channel, electron mobility and interface trap density at high-k/III-V interfaces. A clear change of the dominant scattering mechanism from remote Coulomb scattering to interface roughness scattering at electron density $3x10^{11}$ cm^{-2} was observed. The gated Hall technique can separate the contributions of CB electrons from contribution of the fast traps close to the CB edge. Even the high-quality Al_2O_3/InGaAs interfaces providing high-mobility inversion electron transport suffer from fast border traps that can capture as much as half of the carriers above the CB edge.

REFERENCES

[1] J. A. del Alamo, "Nanometer-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, pp. 317-323, Nov. 2011. DOI: 10.1038/nature10677

[2] P. D. Ye, "Main determinants for III-V metal-oxide-semiconductor field-effect transistors," *J. Vac. Sci. Tech. A*, vol. *26*, no. *4*, pp. 697-704, Jul. 2008. DOI: 10.1116/1.2905246

[3] R. Engel-Herbert, Y. Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces," *J. Appl. Phys.*, vol. *108*, no. 12, pp. 124101, Dec. 2010. DOI: 10.1063/1.3520431

[4] G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, "On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces, " *Appl. Phys. Lett.*, vol. 95, no.20, pp. 202109, Nov.2009. 10.1063/1.3267104

[5] A. Ali, H. Madan, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom, and S. Datta, "Small-Signal Response of Inversion Layers in High-Mobility MOSFETs Made With Thin High-Dielectrics," *IEEE Trans. Electron Dev.*, vol. 57, no.4, pp. 742-748, Mar. 2010. DOI: 10.1109/TED.2010.2041855

[6] C. L. Hinkle, A. M. Sonnet, R. A. Chapman, and E. M. Vogel, "Extraction of the Effective Mobility of MOSFETs," *IEEE Electron Dev. Lett.*, vol. 30, no. 4, pp. 316-318, Mar. 2009. DOI: 10.1109/LED.2009.2012880

[7] A. M. Sonnet, C. L. Hinkle, D. Heh, G. Bersuker, and E. M. Vogel, "Impact of semiconductor and interface-state capacitance on metal/high-k/GaAs capacitance–voltage characteristics," *IEEE Trans. Electron Dev.*, vol. 57, no. 10, pp. 2599-2606, Aug. 2010. DOI: 10.1109/TED.2010.2059029

[8] D. Veksler, G. Bersuker, H. Madan, L. Morassi, G. Verzellesi, "Extraction of interface state density in oxide/III–V gate stacks", *Semiconductor Sci. Technol.*, vol. 30, no.6, pp. 065013, May 2015. DOI: 10.1088/0268-1242/30/6/065013

[9] E. J. Kim, L. Wang, P. M. Asbeck, K. C. Saraswat, and P. C. McIntyre, "Border traps in $Al_2O_3/In_{0.53}Ga_{0.47}As$ (100) gate stacks and their passivation by hydrogen anneals," *Appl. Phys. Lett.*, vol. 96, pp. 012906, Jan. 2010. DOI: 10.1063/1.3281027

[10] Y. Yuan, L. Wang, B. Yu, B. Shin, J. Ahn, P. C. McIntyre, P.M. Asbeck, Mark J. W. Rodwell, Y. Taur, "A distributed model for border traps in Al_2O_3-InGaAs MOS devices," *IEEE Electron Dev. Lett*., vol. 32, no. 4, pp. 485-487, Apr. 2011. DOI: 10.1109/LED.2011.2105241

[11] S. Johansson, M. Berg, K. M. Persson, and E. Lind, "A high-frequency transconductance method for characterization of high-κ border traps in III-V MOSFETs," *IEEE Trans. Electron Dev.*, vol. 60, no. 2, pp. 776-781, Feb. 2013. DOI: 10.1109/TED.2012.2231867

[12] F. F. Fang and A. B. Fowler, "Transport properties of electrons in inverted silicon surfaces," *Phys. Rev.*, vol. 169, no. 3, pp. 619-631, May. 1968. DOI: 10.1103/PhysRev.169.619

[13] L. Morassi, G. Verzellesi, H. Zhao, J. C. Lee, D. Veksler, and G. Bersuker, "Errors Limiting Split-CV Mobility Extraction Accuracy in Buried-Channel InGaAs MOSFETs," *IEEE Trans. Electron Dev.*, vol. 59, no. 4, pp. 1068-1075, Apr. 2012. DOI: 10.1109/TED.2011.2182513

[14] W. Wang, J.C.M. Hwang, Y. Xuan, and P.D. Ye, "Analysis of electron mobility in inversion-mode $Al_2O_3/In_xGa_{1-x}As$ MOSFETs," *IEEE Trans. Electron Dev.*, vol. *58*, no. 7, pp. 1972-1978, Jul. 2011. DOI: 10.1109/TED.2011.2146255

[15] M. Poljak, V. Jovanović, D. Grgec, and T. Suligoj, "Assessment of electron mobility in ultrathin-body InGaAs-on-insulator MOSFETs using physics-based modeling," *IEEE Trans. Electron Dev.*, vol. 59, no. 6, pp. 1636-1643, Jun, 2012. DOI: 10.1109/TED.2012.2189217

[16] N. Taoka, M. Yokoyama, S. H. Kim, R. Suzuki, R. Iida, S. Lee, T. Hoshii, W. Jevasuwan, T. Maeda, T. Yasuda, O. Ichikawa, N. Fukuhara, M. Hata, M. Takenaka, S. Takagi," Impact of Fermi level pinning inside conduction band on electron mobility of $In_xGa_{1-x}As$ MOSFETs and mobility enhancement by pinning modulation", *Appl. Phys. Lett.*, vol. 103, pp. 143509, Oct. 2013. DOI: 10.1063/1.4824474

[17] S. Oktyabrsky, P. Nagaiah, T. Chidambaram, V. Tokranov, M. Yakimov, R. Kambhampati, D. Veksler, G. Bersuker, and N. Goel, "Electron scattering in buried InGaAs/high-κ MOS channels," *ECS Transactions*, vol. *35*, no. 3, pp. 385-395, Jul. 2011. DOI: 10.1149/1.3569931

[18] D. Veksler, P. Nagaiah, T. Chidambaram, R. Cammarere, V. Tokranov, M. Yakimov, Y.-T. Chen, J. Huang, N. Goel, G. Bersuker, C. Hobbs, P. D. Kirsch, and S. Oktyabrsky, "Quantification of interfacial state density (D_{it}) at the high-κ /III-V interface based on Hall effect measurements," *J. Appl. Phys.*, vol. *112*, no. *5*, pp. 054504, Sep, 2012. DOI: 10.1063/1.4749403

[19] T. Chidambaram, D. Veksler, S. Madisetti, A. Greene, M. Yakimov, V. Tokranov, R. Hill and S. Oktyabrsky, "Interface Trap Density and Mobility Extraction in InGaAs Buried Quantum Well Metal-Oxide-Semiconductor Field-Effect-Transistors by Gated Hall Method", *Appl. Phys. Lett.*, v. 104, no.13, pp. 131605, Apr. 2014. DOI: 10.1063/1.4870257

[20] P. Nagaiah, V. Tokranov, M. Yakimov, S. Koveshnikov, S. Oktyabrsky, D. Veksler, W. Tsai, and G. Bersuker, "Mobility and remote scattering in buried InGaAs quantum well channels with high-κ gate oxide," *J. Vac. Sci. Tech. B*, vol. 28, no. 3, pp. 305-309, Jan. 2010. DOI: 10.1116/1.3360903

[21] K. Bhattacharyya, J. Orwa, and S. Goodnick, "Two-dimensional electron transport in selectively doped n-AlGaAs/InGaAs/GaAs pseudomorphic structures," *J. Appl. Phys.*, vol. 73, no. 9, pp. 4396-4403, Jan. 1993. DOI: 10.1063/1.352777

[22] S. Oktyabrsky, V. Tokranov, S. Koveshnikov, M. Yakimov, R. Kambhampati, H. Bakhru, R. Moore, and W. Tsai, "Interface properties of MBE-grown MOS structures with InGaAs/InAlAs buried channel and in-situ high-k oxide," *J. Cryst. Growth*, vol. 311, no. 7, pp. 1950-1953 Mar. 2009. DOI: 10.1016/j.jcrysgro.2008.11.037